

## ELECTRONIC INFORMATION DISCLOSURE STATEMENT

Electronic Version v18

Stylesheet Version v18.0

Title of Invention	Simulating Euclidean wiring directions using Manhattan and diagonal directional wires						
Application Number:	10/043808						
Confirmation Number:	9068						
First Named Applicant:	Steven Teig						
Attorney Docket Number:	SPLX.P0008						
Art Unit:	2818						
Examiner:	Dao H. Nguyen						
Search string:	( 4782193 or 4855253 or 5541005 or 5635736 or 5637920 or 5640327 or 5646830 or 5689433 or 5784289 or 5801385 or 5811863 or 5822214 or 5880969 or 5889329 or 5980093 or 6111756 or 6260183 or 6263475 or 6301686 or 6307256 or 6316838 or 6324674 or 6412097 or 6448591 or 6516455 or 6645842 or 20010009031 or 20020069397 or 20030025205 ).pn.						
<b>US Patent Documents</b>							
Note: Applicant is not required to submit a paper copy of cited US Patent Documents							
init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass
1	1	4782193	1988-11-01	Linsker			
1	2	4855253	1989-08-08	Weber			
1	3	5541005	1996-07-30	Bezama et al.			
1	4	5635736	1997-06-03	Funaki et al.			
1	5	5637920	1997-06-10	Loo			
1	6	5640327	1997-06-17	Ting			
1	7	5646830	1997-07-08	Nagano			
1	8	5689433	1997-11-18	Edwards			
1	9	5784289	1998-07-21	Wang			
1	10	5801385	1998-09-01	Endo et al.			
1	11	5811863	1998-09-22	Rostoker et al.			
1	12	5822214	1998-10-13	Rostoker et al.			

13	5880969	1999-03-09	Hama et al.
14	5889329	1999-03-30	Rostoker et al.
15	5980093	1999-11-09	Jones et al.
16	6111756	2000-08-29	Moresco
17	6260183	2001-07-10	Raspopovic et al.
18	6263475	2001-07-17	Toyonaga et al.
19	6301686	2001-10-09	Kikuchi et al.
20	6307256	2001-10-23	Chiang et al.
21	6316838	2001-11-13	Ozawa et al.
22	6324674	2001-11-27	Andreev et al.
23	6412097	2002-06-25	Kikuchi et al.
24	6448591	2002-09-10	Juengling
25	6516455	2003-02-04	Teig et al.
26	6645842	2003-11-11	Igarashi et al.

## US Published Applications

Note: Applicant is not required to submit a paper copy of cited US Published Applications

init	Cite.No.	Pub. No.	Date	Applicant	Kind	Class	Subclass
dhr	1	20010009031	2001-07-19	Nitta et al.	A1		
dhr	2	20020069397	2002-06-06	Teig et al.	A1		
dhr	3	20030025205	2003-02-06	Shively	A1		

Signature

Examiner Name	Date
<i>Theaw</i>	08/12/04

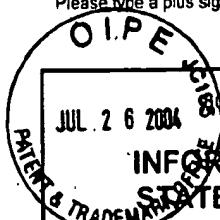
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**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT**

(use as many sheets as necessary)

Sheet	1	of	2	Attorney Docket Number	SPLX.P0008
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**FOREIGN PATENT DOCUMENTS**

Examiner* Initials	Cite No. <sup>1</sup>	Foreign Patent Document		Date of Publication MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T <sup>8</sup>
		Office <sup>3</sup>	Number <sup>4</sup>	Kind Code (if known) <sup>5</sup>			
<i>dhn</i>		1.	JP	04-000677	01-06-1992 Fujiwara et al.	with English translation of Abstract;	
<i>dhn</i>		2.	JP	2000-082743	03-21-2000 Igarashi et al.	with Japanese Patent Office's English translation of Abstract; and with English translation of the application.	✓

**NON PATENT LITERATURE DOCUMENTS**

Examiner* Initials	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.					T <sup>8</sup>
<i>dhn</i>	3.	Chen et al., Optimal Algorithms for Bubble Sort Based Non-Manhattan Channel Routing, May 1994, Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions Volume: 13 Issues, pp. 603-609.					
	4.	Chen, H. et al., Physical Planning of On-Chip Interconnect Architectures, 2002, IEEE, International Conference, pp. 30-35					
	5.	Cong J. et al., DUNE – A Multilayer Gridless Routing System, May 2001, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol 20, iss. 5, pp. 633-647.					
	6.	Dion J. et al., Contour: A Tile-based Gridless Router, March 1995, Digital Western Research Laboratory, research Report 95/3, pp.1-22					
	7.	Morton, P. B. et al., An Efficient Sequential Quadratic Programming Formulation of Optimal Wire Spacing for Cross-Talk Noise Avoidance Routing, UCSC-CRL-99-05, March 10, 1999.					
<i>dhn</i>	8.	NN71091316, Use of Relatively Diagonal And Rectangular Wiring Planes n Multilayer Packages, September 1971, IBM Technical Disclosure Bulletin, Vol. No. 14, Issue No. 4, pp. 1316-1317.					

Examiner Signature	<i>Roas</i>	Date Considered	08/12/04
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## INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet	2	of	2	Application Number	10/043,808
				Filing Date	1/11/2002
				First Named Inventor	Steven Teig
				Group Art Unit	2818
				Examiner Name	Dao Nguyen
				Attorney Docket Number	SPLX.P0008

## NON PATENT LITERATURE DOCUMENTS

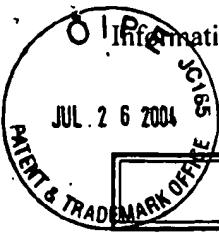
Examiner* Initials	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	<sup>2</sup>
dha	9.	Royle, J. et al., Geometric Compaction in One Dimension for Channel Routing, 24 <sup>th</sup> ACM/IEEE Design Automation Conference, 1987, pp 140-145.	
dha	10.	Schiele, W. et al., A Gridless Router for Industrial Design Rule, 27 <sup>th</sup> ACM-IEEE Design Automation Conference, pp. 626-631, 1990.	
dha	11.	Tseng H. et al., A Gridless Multilayer Router for Standard Cell Circuits Using CTM Cells, Oct. 1999, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol 18, iss. 10, pp. 1462-1479.	

Examiner Signature	Kao	Date Considered	08/12/04
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	16	6111756	2000-08-29	Moresco	
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	19	6301686	2001-10-09	Kikuchi et al.	B1
	20	6307256	2001-10-23	Chiang et al.	B1
	21	6316838	2001-11-13	Ozawa et al.	B1
	22	6324674	2001-11-27	Andreev et al.	B2
	23	6412097	2002-06-25	Kikuchi et al.	B1
	24	6448591	2002-09-10	Juengling	B1
	25	6516455	2003-02-04	Teig et al.	B1
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dhr	2	20020069397	2002-06-06	Teig et al.	A1		
dhr	3	20030025205	2003-02-06	Shively	A1		

## Signature

Examiner Name	Date
	08/04/04